In The Specification:

Please amend the first paragraph on page 2 as follows:

Referring to Fig. 1, an air gap 106 is formed in a dielectric layer between the conducting wires 102 on a substrate 100 in order to reduce the capacitive and inductive couplings between the multilevel interconnects. As the air has a smaller dielectric constant (about 1), the inter-metal dielectric (IMD) made with the air gap between the multilevel interconnects can reduce the dielectric constant and the capacitance between the parallel conducting wires, while improving the data transmission speed and the device efficiency.

Please amend the paragraph beginning at page 5, line 6, as follows:

Fig. 3A is schematic diagram illustrating the via opening when misalignment occurs.

Please amend the paragraph beginning at page 5, line 8, as follows:

Fig. 3B [[~~3A~~]] is schematic diagram illustrating another interconnect structure according to the first preferred embodiment of the invention;

Please amend the paragraph beginning at page 8, line 17, as follows:

Referring to Fig. 3A, if a misalignment occurs during the formation of the opening, a misaligned opening 312 is formed. The opening 312 is shifted to the gap region. In Fig. 3A, the elements with the same reference numbers represent the same elements in Fig. 2E. Since the anti-etch layer 207a has a smaller etching rate relative to the dielectric layer 204. In other words, the anti-etch layer 207a is a mask layer serving as an etching stop. As a result, the portion of the opening 312 above the gap region stops on the anti-etching layer 207a or just an upper portion of the anti-etching layer 207a being etched without opening the void 206. The void 206 reduces the parasitic capacitance in the inter-metal dielectric layer of the interconnecting structure.

Please amend the paragraph beginning at page 9, line 3, follows:

Fig. 3B [[~~3A~~]] is schematic diagram illustrating another interconnect structure according to the first preferred embodiment of the invention. The anti-etch layer 207b over the void 206 is formed by directly patterning the anti-etch layer by an additional photolithography step. In this manner, the geometric structure of the anti-etch layer 207b is different and met requirements of designs. Furthermore, it can also be a damascened layer in the dielectric layer 204 over the void 206.